BROADBAND 50 WATT CW RECEIVER PROTECTOR USING GLASS INTEGRATED CIRCUIT TECHNOLOGY

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Abstract

This paper describes a passive glass microwave integrated circuit providing passive limiting and active switching from 2 - 8 GHz. The 0.265" x 0.100" chip employs discrete PIN diodes to achieve the following performance:

Loss:	0.5 dB
VSWR:	1.30:1
Isolation:	45 dB
Power Handling:	50 W CW
Leakage:	20 dBm

Introduction

Solid state phased array radar systems find use in an increasing number of applications. Modern phased array radar systems contain many thousand of channels. Each channel has transmit and receive capability. The receive channel contains components that high power signals will damage.

The high power signals can come from two sources. The isolation of the source from the receiver channel is finite. This ensures that transmit power will leak into the receive channel. The occurrence of this event is predictable, so an active switching function can protect the receiver from damage. If unpredictable high power signals are present, a signal at the antenna may be high enough to damage the receiver channel. Since the system may not be in operation during this time, this protection must be passive.

This paper describes a 2 - 8 GHz integrated circuit design that performs the active switching and passive limiting function for very high levels of incident CW power. The circuit is fabricated using M/A-COM's glass integrated circuit process. The process allows the repeatability and reliability benefits of an integrated circuit process with the power performance advantages of a discrete design.

This glass process combines a single crystal Silicon wafer with a wafer of sealing glass. Silicon vias that extend to the top surface of the chip provide thermal and electrical ground for discrete components. The highly doped Silicon wafer provides low thermal and electrical resistance for superior power handling. The glass wafer is a low loss dielectric that readily accepts thinfilm batch processing techniques. The completed integrated circuit contains transmission lines, spiral inductors, airbridges and MIM capacitors. Discrete PIN diodes are mounted to the glass chip to achieve this limiting function.

Design

The function of a receiver protector is to provide protection for components that high incident power levels will damage. As input power increases, the PIN diodes will experience conductivity modulation. This will reduce the forward resistance of the diode to very low levels. Even at the highest input powers, there is some residual resistance. This resistance results in a portion of the input power being dissipated in the diode. The amount of dissipation and the total thermal resistance path determine the power handling capability.

Power dissipated in the PIN diode manifests itself as heat. Studies report the migration of gold atoms from the P to the N region of the PIN diode above 300 °C. This creates a permanent low resistance path, causing

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the diode to fail. For the case of a CW input signal, the increase in junction temperature is given by:

$$T_{inc} = P_{diss} \times \Theta_{cw} \qquad (1)$$

Where: T_{inc} = Junction temperature increase (°C)
P_{diss} = Dissipated power (Watts)
Θ_{cw} = Thermal Resistance (°C/W)

The geometry of a PIN diode determines the thermal resistance. PIN diodes with larger intrinsic regions (higher breakdown voltages) have lower thermal resistances. Unfortunately, this larger geometry results in higher junction capacitance. To circumvent this problem, this design uses a dual junction plated heat sink diode. Each junction of this dual diode has a 45 μm I-region thickness (nominally a 350 Volt breakdown level). The plated heat sink structure enables the diode to achieve a thermal resistance of 10^0C/W with a total junction capacitance of less than 0.15 pF.

The total thermal resistance path includes the mounting configuration, as well as the diode. The structure of this glass chip is also advantageous in this area. As described, highly doped single crystal Silicon via structures extend from the ground plane of the chip to the surface. This highly doped Silicon via has a calculated thermal impedance of 2-3^{0}C/W. This feature makes this an attractive integrated circuit medium for high power applications.

The 50 Watt CW power handling requirement is the driver for the electrical design. To provide passive and active protection, the device must function as a passive limiter and an SPST when actively biased. A Schottky coupled limiter section fulfills both design requirements.

In the passive condition with increasing incident power, the coupled portion of the power forward biases the Schottky and completes the current loop. This, in turn, forward biases the PIN limiter diodes to provide protection. During active operation, the receiver protector is externally biased. With a positive voltage, the Schottky diode is reverse biased and the PIN diodes are forward biased. This is the isolation state. Insertion loss is achieved with a 0 volt bias, keeping the Schottky and PIN diodes reverse biased at the operating power levels. The schematic for the receiver protector is shown in Figure 1.

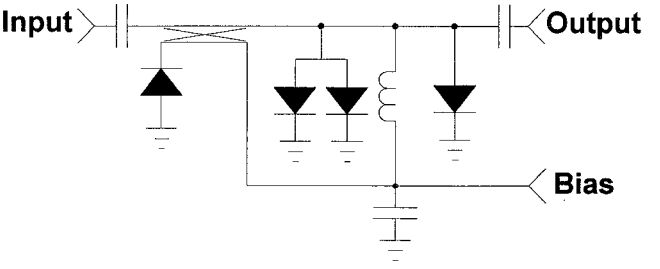

Figure 1: Receiver Protector Schematic

A two stage limiter design achieves the power handling and leakage requirements. The input stage is the dual junction plated heat sink diode described earlier. The coupler, nominally 25 to 30 dB, provides power to the Schottky, resulting in enough current to saturate the limiter section. The second stage is a 2 to 3 μm I-region (25V-30V breakdown). The Schottky diode is a low barrier from M/A-COM's Semiconductor Business Unit.

The completed chip is 0.265" x 0.100" x .015". The glass portion is .008" thick with .007" of backside Silicon. A photograph of the completed receiver protector chip is shown in Figure 2.

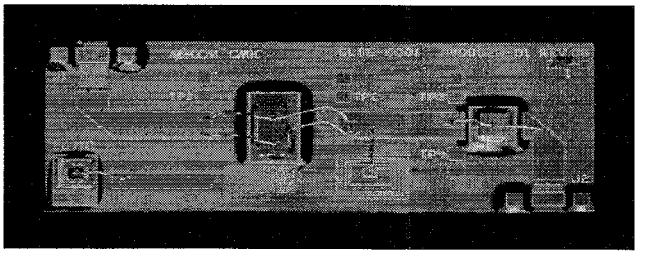

Figure 2: Glass Receiver Protector Chip

The photo shows the input dual diode, the clean-up diode and the Schottky diode as the only discrete components on the chip. All the other circuit structures are fabricated during the batch processing of the glass wafer.

Results

The following low power plots are from a representative sample of eight units. The data illustrates the repeatability that results from an integrated circuit process.

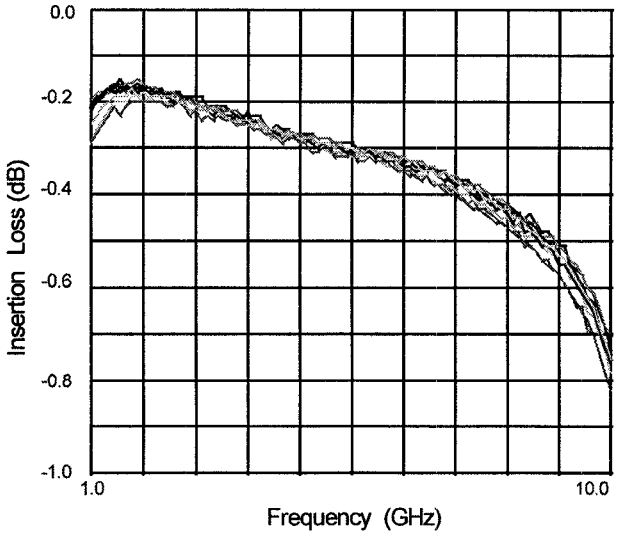

Figure 3: Insertion Loss vs. Frequency

Figure 3 shows the extremely low loss, broadband behavior of this device. The insertion loss stays well below 1 dB, at room temperature, from 2 to 10 GHz. The receiver protector is typically located before a low noise amplifier, so the insertion loss of the device contributes directly to the channel noise figure. Over the desired band, the insertion loss is below 0.5 dB.

Figure 4 also illustrates the broadband nature of the design. The operational bandwidth is extended by using fifty ohm transmission line. The inductances and capacitances of the discrete elements and circuit can be combined with transmission elements to form a band pass filter structure. This decreases overall size at the expense of bandwidth. This tuning technique can also be used to improve the return loss and, subsequently, the insertion loss of the device. In this case, the goal was for maximum bandwidth.

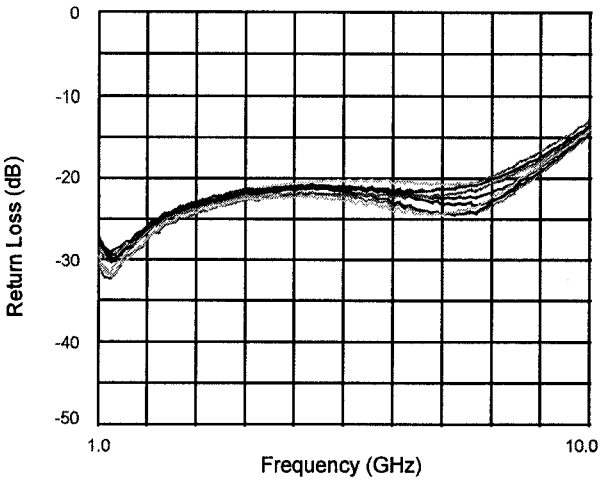

Figure 4: Return Loss vs. Frequency

The final low power performance characteristic is illustrated in Figure 5. The isolation characteristic is important during active switching when the radar is on and the switch is biased. During this period, the isolation determines the level of transmitter leakage that is incident on the receiver. The accompanying plot shows the isolation is flat over the desired bandwidth at a value typically much greater than 45 dB.

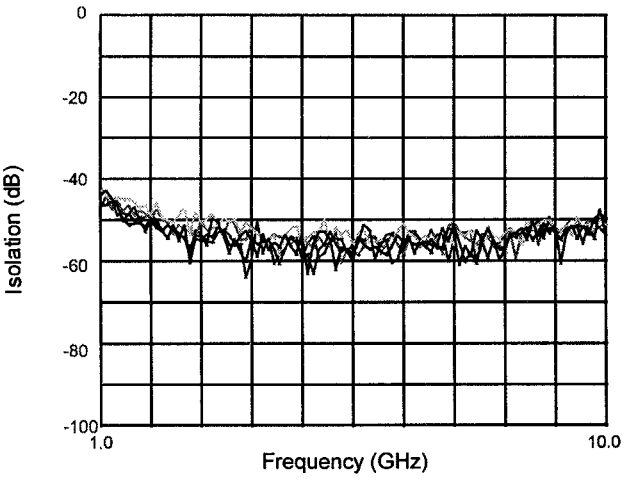

Figure 5: Isolation vs. Frequency

Figure 6 illustrates the high power performance of the receiver protector. The measurements were taken on a CW signal at 4 GHz. The response illustrates the characteristic behavior of a Schottky coupled limiter. Over the initial input power ranges (up to approximately 15 dBm), the output power stays fairly linear with input power increase. Above these power levels, the diodes start to compress until the input power reaches 28 - 30 dBm. At this level, the power coupled to the Schottky creates sufficient current to dramatically decrease the resistance of the limiter diodes, increasing the loss of the device. At the highest power levels, the diodes are saturated, so the output power again becomes linear with the input power.

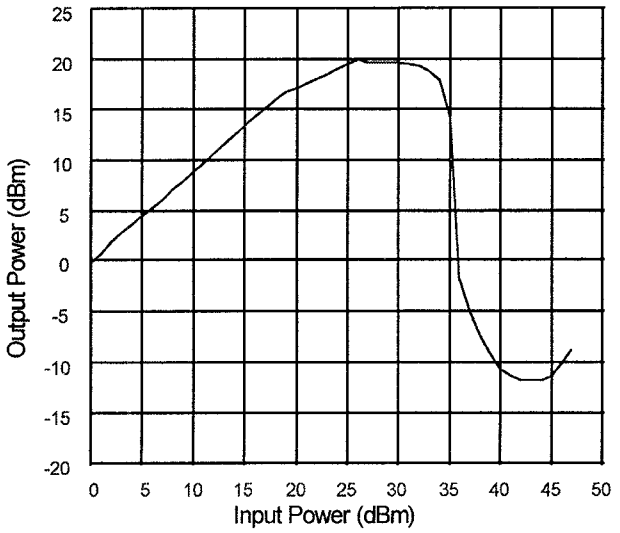

Figure 6: Output Power vs. Input Power

Summary

This paper describes the design and test results of a receiver protector for phased array radar applications. This receiver protector is fabricated using a glass integrated circuit process that offers the advantages of thinfilm batch processing techniques with the power performance advantages of a discrete design. The design and processing techniques result in a small (0.265" x 0.100") chip that will handle up to 50 watts CW over the 2 - 8 GHz frequency range with insertion loss less than 0.5 dB.

References and Further Reading

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